Ethan Huang

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EDUCATION

Georgia Institute of Technology Atlanta, GA

Bachelor of Science in Electrical Engineering **– GPA: 4.0** *Aug 2024 – Dec 2027*

Concentration: Signal Processing and Circuit Technology

WORK EXPERIENCE

Apple, Design Verification Internship, *Cupertino, CA* *May 2026 – August 2026*

- Incoming DV intern at Apple.

Flavin Neuromachines Lab, Undergraduate Researcher, *Atlanta, GA* *May 2025 – Present*

- Architected novel methods to validate and characterize code generated by a Large Language Model.
- Integrated these methods into a flow to prove whether the generated code matches user intent from any arbitrary prompt.

Plasma and Dielectrics Laboratory, Undergraduate Researcher, *Atlanta, GA* *Feb 2025 – Present*

- Manufactured a custom PCB so it can do a double-pulse characterization of a four-quadrant switch under cryogenic environments.
- Co-authored "Characterization of an 850 nm Power-over-Fiber Converter at Cryogenic Temperatures".

ACTIVITIES

SiliconJackets, Design Verification/Emulation Lead, *Atlanta, GA* *Aug 2024 – Present*

- Leading the Design Verification team, developing testbenches, reviewing members' work, and mentoring team members.
- Spearheaded UVM adoption across the team by creating onboarding materials and supplementary notes.
- Creating our regression testing flow.

RoboJackets, Electrical Engineer, *Atlanta, GA* *Aug 2024 – Present*

- Designed a STM32 microcontroller board to replace a Teensy, with USB-C support for programming, integrated power muxing, and expanded I/O capability.
- Redesigned the motor board by replacing hand-soldered fixes with proper additional components, separated clock/UART buses, optimized layout for mechanical constraints, and improved debug access.

PROJECTS

An Open-Source Digital Delay Locked Loop for Educational and Architectural Exploration *Feb 2026 – Apr 2026*

- Led team development, managing tasks and documenting work in a technical notebook.
- Characterized and analyzed Delay Locked Loop (DLL) subcomponent variations using SPICE simulations.
- Developed a high-level Python model of DLL behavior, enabling rapid evaluation and comparison of component trade-offs.

Dynamically Pipelined Arithmetic Modules for Adaptive Critical Path Optimization *Feb 2025 – Apr 2025*

- Built a retiming engine which increased the clock speed of custom arithmetic modules by 30%.
- Presented this at the 2025 Symposium on VLSI Technology and Circuits.

SKILLS

Programming: SystemVerilog, Python, JavaScript, C, C++

Tools: VCS, Verdi, Xcelium, IMC, SimVision, Openlane, KiCAD, LTspice

Skills: Design Verification, UVM, Regression Testing, Signal Processing, Digital Design, PCB Design, Soldering

HONORS AND AWARDS

IEEE SSCS Code-a-Chip Travel Grant Award June 2025

Coursera Machine Learning Specialization April 2023

Coursera Mathematics for Machine Learning April 2022